IN THE CLAIMS:

Please cancel claim 33 without prejudice, amend claims 1 and 8-29, and add new claims 65-82, all as follows:

1. (Amended) An integrated circuit comprising:

circuitry comprising a first part and a second part;

a bond pad directly coupled to the first part of the circuitry and for interfacing the circuitry with an external circuit; and

a special contact pad directly coupled to the second part of the circuitry, the special contact pad for use only when testing the circuitry.

2. (Original) The integrated circuit of claim 1, wherein the special contact pad is smaller than the bond pad.

3. (Original) The integrated circuit of claim 1, wherein the special contact pad has a maximum dimension of approximately 10 microns.

4. (Original) The integrated circuit of claim 1, wherein the special contact pad is structured to receive a spring contact element.

5. (Original) The integrated circuit of claim 1, wherein the special contact pad is for communicating test data to the circuitry.

6. (Original) The integrated circuit of claim 1, wherein the special contact pad is for communicating data from the circuitry.

7. (Original) The integrated circuit of claim 1, wherein the special contact pad is for contacting a circuit node internal to the circuitry.

8. (Amended) An integrated circuit comprising:

a ~~plurality of circuits~~ first circuit;

a second circuit;

a ~~plurality of~~ bond ~~pads each~~ pads coupled to ~~at least one of~~ the ~~plurality of circuits~~ first circuit, the ~~plurality of bond pads~~ bond pad for interfacing the ~~plurality of circuits~~ first circuit with ~~circuits~~ a circuit external to the integrated circuit; and

a ~~plurality of~~ special contact ~~pads each~~ pads coupled to ~~at least one of~~ the ~~plurality of circuits~~ second circuit ~~and providing an electrical contact for communicating with the plurality of circuits,~~

wherein the special contact pad is smaller than the bond pad.

9. (Amended) The integrated circuit of claim ~~8~~ 13, wherein the bond pads are arranged in a first predetermined alignment and the special contact pads are arranged in a second predetermined alignment.

10. (Amended) The integrated circuit of claim ~~8~~ 13, wherein the bond pads are disposed along the periphery of the integrated circuit, and at least one of the special contact pads is not disposed on the periphery of the integrated circuit.

11. (Amended) The integrated circuit of claim ~~8~~ 13, wherein the bond pads are aligned in a grid pattern on the integrated circuit, and at least one of the special contact pads is not aligned in the grid pattern.

12. (Amended) The integrated circuit of claim ~~8~~ 13, wherein the bond pads are aligned in a lead-on-center configuration, and at least one of the special contact pads is not aligned in the lead-on-center configuration.

13. (Amended) The integrated circuit of claim 8~~, wherein the special contact pads are smaller than the bond pads~~ further comprising:

a plurality of the first circuits;

a plurality of the second circuits;

a plurality of the bond pads, each coupled to at least one of the plurality of first circuits; and

a plurality of the special contact pads each coupled to at least one of the second circuits.

14. (Amended) The integrated circuit of claim 8, further comprising a spring contact element attached to ~~one of~~ the special contact ~~pads~~ pad.

15. (Amended) The integrated circuit of claim ~~8~~ 13, wherein at least one of the special contact ~~pad~~ pads is electrically disposed between two of the ~~plurality of~~ circuits to monitor signals transmitted between the two circuits.

16. (Amended) The integrated circuit of claim ~~8~~ 13, wherein one of the special contact pads communicates test data to one of the circuits, and another one of the special contact pads communicates an output of the circuit.

17. (Amended) The integrated circuit of claim ~~8~~ 13, wherein one of the special contact pads communicates test data to the one of the circuits, and one of the bond pads communicates an output of the circuit.

18. (Amended) The integrated circuit of claim ~~8~~ 13, wherein one of the bond pads communicates test data to one of the circuits, and one of the special contact pads communicates an output of the circuit.

19. (Amended) The integrated circuit of claim 8, wherein in a first mode of operation ~~one of~~ the special contact pads communicates data to ~~one of~~ the ~~circuits~~ second circuit, and in a second mode of operation the special contact pads communicates data from the second circuit.

20. (Amended) The integrated circuit of claim 8, wherein ~~one of the plurality of circuits~~ the second circuit is an embedded memory array, and the special contact pads communicates address and test data to the embedded memory array.

21. (Amended) The integrated circuit of claim 8, wherein ~~one of the plurality of circuits~~ the second circuit includes programmable circuitry, and the special contact ~~pads are~~ pad is for communicating signals for programming the programmable circuitry.

22. (Amended) The integrated circuit of claim 8, wherein the bond ~~pads are~~ pad is structured to be connected to external circuitry by a bonding ~~wires~~ wire, and the special contact ~~pads are~~ pad is not structured to be connected to external circuitry by a bonding ~~wires~~ wire.

23. (Amended) The integrated circuit of claim 8, wherein the bond ~~pads are~~ pad is structured to be connected to external circuitry by solder bumps, and the special contact ~~pads are~~ pad is not structured to be connected to external circuitry by a solder ~~bumps~~ bump.

24. (Amended) The integrated circuit of claim 8, wherein the bond ~~pads are~~ pad is structured to be in electrical contact with a package for housing the integrated circuit, and the special contact ~~pads are~~ pad is not structured to be in electrical contact with the package.

25. (Amended) The integrated circuit of claim 8, ~~wherein the plurality of circuits includes a first circuit and a second~~ further comprising

a third circuit having a redundant function of the ~~first~~ second circuit, and

~~wherein~~ a plurality of the special contact pads ~~are~~ disposed about the ~~first and~~ second and third circuits to communicate with the ~~first and~~ second and third circuits.

26. (Amended) The integrated circuit of claim 25, further comprising means for communicating with the special contact pads and for disabling the ~~first~~ second circuit if it is defective and for enabling the ~~second~~ third circuit.

27. (Amended) The integrated circuit of claim 25, further comprising means for communicating with the special contact pads and for disabling the ~~second~~ third circuit.

28. (Amended) The integrated circuit of claim 8, further comprising electrostatic discharge protection circuitry for the bond ~~pads~~ pad and not for the special contact ~~pads~~ pad.

29. (Amended) An integrated circuit comprising:

a plurality of bond pads;

an internal circuit not directly monitorable by the bond pads; and

at least one special contact pad for directly accessing the internal circuit, wherein said at least one special contact pad is smaller than each of said bond pads.

30. (Original) The integrated circuit of claim 29, wherein the internal circuit comprises an embedded memory array, and the at least one special contact pad communicates address and memory data with the embedded memory array.

31. (Original) The integrated circuit of claim 29, wherein the internal circuit comprises programmable circuitry, and the at least one special contact pad communicates programming signals to the programmable circuitry.

32. (Original) The integrated circuit of claim 29, wherein the bond pads are arranged in a first predetermined alignment and the at least one special contact pad is in a second predetermined alignment.

Claim 33 (cancelled).

34. (Original) The integrated circuit of claim 29, further comprising a spring contact element attached to the at least one special contact pad.

Claims 35-64 (cancelled).

65. (New) The integrated circuit of claim 8, wherein the first circuit is coupled to the second circuit.

66. (New) An integrated circuit comprising:

a first input/output buffer circuit;

a second input/output buffer circuit smaller than said first input/output buffer circuit;

a first contact structure electrically connected to said first input/output buffer circuit; and

a special contact structure electrically connected to said second input/output buffer circuit.

67. (New) The integrated circuit of claim 66 further comprising:

first discharge protection means for protecting said integrated circuit from electrostatic discharge through said first contact structure, said first discharge protection means sized to protect against electrostatic discharge up to a first level of discharge; and

second discharge protection means for protecting said integrated circuit from electrostatic discharge through said special contact structure, said second discharge protection means sized to protect against electrostatic discharge up to a second level of discharge,

wherein said second level of discharge is less than said first level of discharge.

68. (New) The integrated circuit of claim 66, wherein said special contact structure is smaller than said first contact structure.

69. (New) The integrated circuit of claim 66, wherein said first contact structure and said special contact structure are disposed on a surface of said integrated circuit, and a height of said special contact structure from said surface is less than a height of said first contact structure from said surface.

70. (New) The integrated circuit of claim 66, wherein said first contact structure is adapted to provide electrical connections between said first input/output buffer circuit and a printed circuit board.

71. (New) The integrated circuit of claim 66 further comprising:

a plurality of said first input/output buffer circuits; and

a plurality of said first contact structures.

72. (New) The integrated circuit of claim 71 further comprising:

a plurality of said second input/output buffer circuits; and

a plurality of said special contact structures.

73. (New) An integrated circuit comprising:

first discharge protection means for protecting said integrated circuit from electrostatic discharge, said first discharge protection means sized to protect against electrostatic discharge up to a first level of discharge;

second discharge protection means for protecting said integrated circuit from electrostatic discharge, said second discharge protection means sized to protect against electrostatic discharge up to a second level of discharge, wherein said second level of discharge is less than said first level of discharge;

a first contact structure electrically connected to said first electrostatic discharge protection means; and

a special contact structure electrically connected to said second electrostatic discharge protection means.

74. (New) The integrated circuit of claim 73, wherein said special contact structure is smaller than said first contact structure.

75. (New) The integrated circuit of claim 73, wherein said first contact structure and said special contact structure are disposed on a surface of said integrated circuit, and a height of said special contact structure from said surface is less than a height of said first contact structure from said surface.

76. (New) The integrated circuit of claim 73 further comprising a plurality of said first contact structures.

77. (New) The integrated circuit of claim 76 further comprising a plurality of said special contact structures.

78. (New) An integrated circuit comprising:

an input/output driver circuit;

a first circuit block;

a second circuit block that is redundant of said first circuit block;

selecting means for selecting one of said second circuit block or said first circuit block;

a first contact structure electrically connected to said input/output driver circuit; and

a special contact structure electrically connected to said selecting means.

79. (New) The integrated circuit of claim 78, wherein said special contact structure is smaller than said first contact structure.

80. (New) The integrated circuit of claim 78, wherein said first contact structure and said special contact structure are disposed on a surface of said integrated circuit, and a height of said special contact structure from said surface is less than a height of said first contact structure from said surface.

81. (New) The integrated circuit of claim 78 further comprising an additional special contact structure electrically connected to said first circuit block for monitoring operation of said first circuit block.

82. (New) The integrated circuit of claim 78 further comprising a plurality of said first contact structures.